Power Crystal Oscillator With Feedback Stabilized Duty Cycle

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Most crystal oscillators suffer from three drawbacks, they can't drive much of a load, the duty cycle is not adjustable, and the duty cycle drifts. This crystal oscillator circuit solves these problems: three parallel gates drive heavy loads (inverters can be used if the enable function isn't required), the duty cycle is adjustable from 25% to 75%, and drift is minimized by feedback.

The oscillator circuit consists of C_1, C_2, C_3, R_1, R_2, R_{10}, one gate and the crystal. R_1 and R_{10} bias the gate in its linear region, while the capacitors form a π filter around the crystal. The π network preserves the crystal's Q, provides the correct loading capacitance for the crystal, and prevents oscillations at spur frequencies. R_2 limits the crystal's power dissipation to 5mW. The difference between the output voltage (3.9V) and the input voltage (2V) is about 1.9V (Typical TTL threshold voltage), so although it is an optimistic approximation, Equation 1 can be used to select R_2.

$$R_2 \geq \frac{1.9^2}{P_{CRYSTAL}} = \frac{1.9^2}{5}K = 722\Omega \quad \text{(EQ. 1)}$$

FOR $P_{CRYSTAL}$ = 5mW, SELECT $R_2 = 750\Omega$

R_2 and C_3 form a low pass filter whose -3dB point should be set at $f_{OSC}/8$ or higher, this choice prevents spurious high frequency oscillations. The -3dB point for this design is selected as $f_{OSC}/8$ = 625kHz. C_3 is calculated from Equation 2.

$$C_3 = 1/_{2\pi f R_2} = 1/_{2\pi(6.25)(10^5)(750)} = 339pF \approx 300pF \quad \text{(EQ. 2)}$$

C_1 must be a large value to minimize the effects of stray capacitance changes, so C_1 is selected as 510pF. The series combination of C_1, C_2, and C_3 must equal the specified load capacitance for a parallel resonant crystal so:

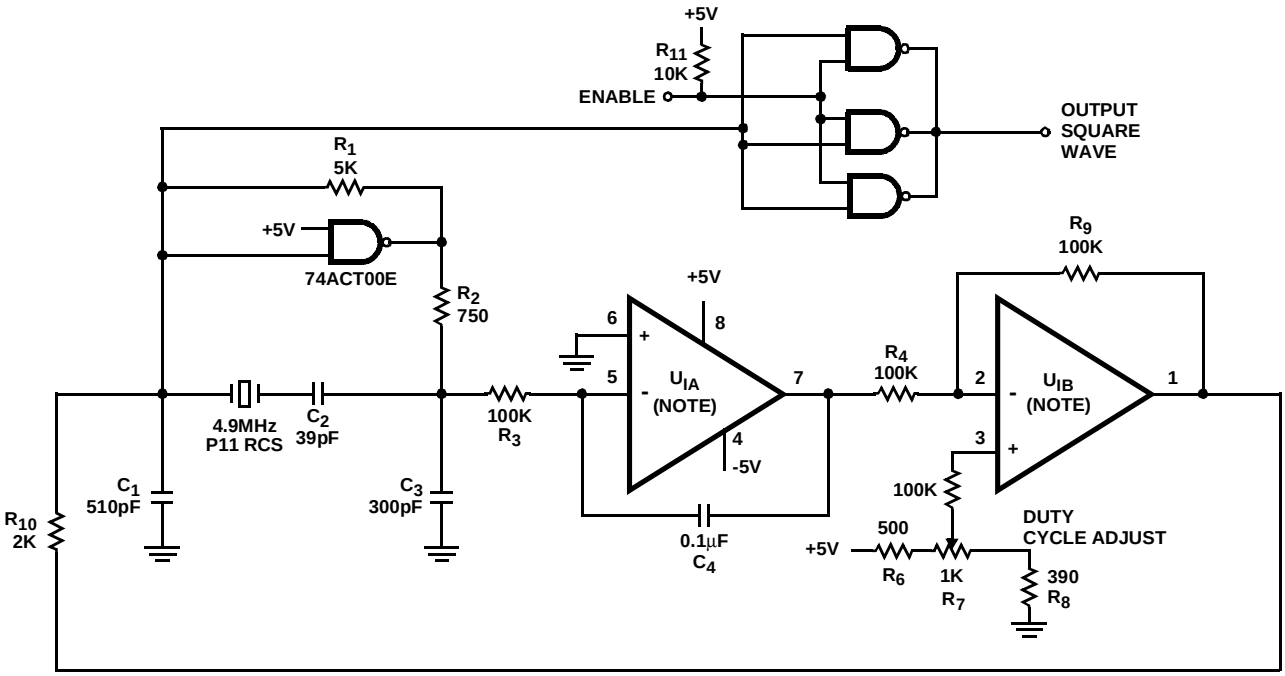
$$1/_{C_2} = 1/_{C_L} - 1/_{C_1} - 1/_{C_3} \quad \text{(EQ. 3)}$$

The load capacitance for the selected crystal is 32pF, requiring a C_2 of 38.5pF, thus C_2 is selected as 39pF. With the component values shown, the circuit oscillates at 5MHz with a parallel resonant crystal. The duty cycle is a function of the gate bias point resistors, therefore variations in logic gates cause variations in duty cycle, typically 30% to 65% with normal manufacturing tolerances. The duty cycle adjustment compensates for this variation, and the feedback provided by the op amps reduces drift to a fraction of a percent.

U_{1A} integrates the oscillator output into a DC level. The ICL7621A was chosen for this function because it has high input impedance, large output swing, and it functions with a 5V supply. U_{2A} sums the integrated signal with the duty cycle set point voltage to create an error signal. The feedback loop keeps the duty cycle constant by changing the oscillator gate bias point until the error signal reaches zero.

The output gates are paralleled for increased drive capability. All gates are in the same IC so they can safely be paralleled, and the oscillator/output gate delays will match well under reasonable loading. The enable input gates the oscillator output when required with just a gate delay. Gating the oscillator by turning it off/on incurs an oscillator start-up delay which is microseconds or longer. Replace the NAND gates with inverters when the enable function is not used.

If the output loading changes during operation, the feedback point can be taken from the output to compensate for varying loads. Beware, ringing resulting from poorly terminated transmission lines can cause duty cycle variations when the feedback point is taken from the output. If minimizing duty cycle drift is not important, feedback is not required, so R_{10} can be split into a 2.5K fixed and a 5K variable resistor connected to ground. This selection of R_{10} enables 25% to 75% duty cycle adjustment. For different logic families you must verify, and possibly reselect, the gate bias resistors.



NOTE: $^1/_2$ of ICL7621A

FIGURE 1. POWER CRYSTAL OSCILLATOR WITH FEEDBACK STABILIZED DUTY CYCLE

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